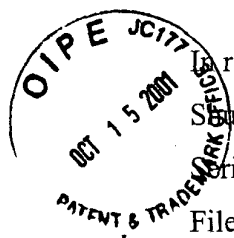


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



Large Patent Application of )  
Shunpei YAMAZAKI et al. ) Attention: Applications Branch  
Serial No. 09/837,558 )  
Filed: April 19, 2001 )  
For: SEMICONDUCTOR DEVICE AND )  
MANUFACTURING METHOD )  
THEREOF )

**RESPONSE TO NOTICE OF INCOMPLETE REPLAY**  
**AND PRELIMINARY AMENDMENT**

Honorable Commissioner for Patents  
Washington, D.C. 20231  
Sir:

In response to the Notice of Incomplete Reply – Filing Date Granted dated October 9, 2001 please preliminary amend the above-identified application as follows:

**IN THE CLAIMS:**

Please cancel claims 1-16 and add new claims 17-32 as follows:

--17. A semiconductor device including a CMOS circuit formed by n-channel TFT and p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first wiring line and a second wiring line through an insulating layer in the n-channel TFT,

the active layer includes a low concentration impurity region that is in contact with the channel formation region; and

the low concentration impurity region is formed to overlap the first wiring line and not to overlap the second wiring line.

18. A semiconductor device including a CMOS circuit formed by n-channel TFT and p-channel TFT, characterized in that:

the CMOS circuit has a structure that an active layer is sandwiched by a first